CLAIMS

1. A method of fabricating an integrated circuit device comprising:

providing an opening in an insulating layer of a partially completed device to a lightly doped diffusion region; and

providing a conductor in said opening and in contact with said lightly doped diffusion region, said conductor having a first conductive layer with a first dopant and a first dopant concentration, and a second conductive layer on said first conductive layer; said second conductive layer having a second dopant at a second dopant concentration.

2. The method of claim 1 wherein providing said conductor comprises depositing said first conductive layer.

3. The method of claim 1 wherein providing said conductor comprises depositing said second conductive layer on said first conductive layer.

4. The method of claim 1 wherein providing said conductor comprises implanting said first dopant in said first conductive layer.

5. The method of claim 1 wherein providing said conductor comprises implanting said second dopant in said second conductive layer.

6. The method of claim 2 wherein depositing said first conductive layer includes providing said first dopant in situ.

7. The method of claim 2 further comprises dry etching said first conductive layer to a desired thickness.

8. The method of claim 2 wherein depositing said first conductor layer comprises lining said opening with said first conductor layer.

9. The method of claim 2 further comprising depositing said second conductive layer with said first dopant in situ on said first conductive layer.

10. The method of claim 2 further comprising depositing said second conductive layer on said first conductive layer, and implanting said first dopant in said first conductive layer through said second conductive layer.

11. The method of claim 3 wherein depositing said second conductive layer includes said second dopant in situ.

12. The method of claim 7 further comprises depositing said second conductive layer over said first conductor layer.

13. The method of claim 7 wherein depositing said first conductive layer includes said first dopant in situ.

14. The method of claim 7 further comprising implanting said first dopant in said first conductive layer.

15. The method of claim 9 further comprising implanting said second dopant in said second conductive layer.

16. The method of claim 9 wherein depositing said second conductive layer includes said second dopant in situ.

17. The method of claim 12 further comprising implanting said second dopant in said second conductive layer.

18. The method of claim 12 wherein depositing said second conductive layer includes said second dopant in situ.

19. The method of claim 1 wherein said first dopant diffusivity is less than said second dopant.

20. The method of claim 1 further comprising forming by solid state diffusion a shallow diffusion region in said lightly doped diffusion region beneath said conductor having a dopant concentration greater than said lightly doped diffusion region.

21. The method of claim 20 further comprising forming by solid state diffusion a graded dopant concentration in a portion of said lightly doped diffusion region by diffusing below and adjacent said shallow diffusion region.

22. The method of claim 1, wherein said first dopant comprises arsenic, antimony, or combinations thereof, and said second dopant comprises phosphorus.

23. The method of claim 1, wherein said first and second dopants each comprises boron, BF_2, borane, or combinations thereof.

24. The method of claim 1, wherein said first dopant concentration is from about 1 E 19 ions/cm^3 to about 1 E 21 ions/cm^3.

25. The method of claim 1, wherein said second dopant concentration is from about 1 E 19 ions/cm^3 to about 1 E 21 ions/cm^3.

26. The method of claim 20, wherein said shallow diffusion region extends beneath said conductor to a depth less than about 0.02μm.

27. The method of claim 1, wherein providing said conductor includes providing said first conductive layer to a thickness of from about 100 to about 1000 Angstroms.

28. The method of claim 1, wherein providing said conductor includes proving said second conductive layer to a thickness of from about 2000 to about 2500 Angstroms.

29. The method of claim 7, wherein said depositing said first conductive layer includes depositing said first conductive layer to a thickness about 15% larger that said desired thickness of from about 100 to about 1000 Angstroms.

30. The method of claim 4, wherein implanting said first dopant is at dosages of between about 1 E 14 to about 1 E 16 atoms/cm^2 and at energies of between about 1 to about 15 KeV at a vertical angle to provide an average dopant concentration for first conductive layer of from about 1 E 19 ions/cm^3 to about 1 E 21 ions/cm^3.

31. The method of claim 5, wherein implanting said second dopant is at a dosage between about 1 E 14 to about 1 E 16 atoms/cm^2 and at energies of between about 1 to about 15 KeV at a vertical angle to provide an average dopant concentration for the second conductive layer of from about 1 E 19 to about 1 E 21 ions/cm^3.

32. A method of fabricating an integrated circuit device comprising:

providing a layer of a field oxide over the surface of a semiconductor substrate;

forming a gate electrode overlying said field oxide layer;

forming a capping layer having sidewalls on the surface and sidewalls of said gate electrode;

providing lightly doped source/drain regions in said semiconductor substrate adjacent said gate electrode;

forming spacers on sidewalls of said capping layer;

providing an insulating layer over the surface of said substrate;

providing an opening through said insulating layer to one of said lightly doped source/drain regions;

providing a first conductive layer in said opening and in contact with said one of said lightly doped source/drain regions, said first conductive layer having a first dopant and a first dopant concentration,

providing a second conductive layer on said first conductive layer; said first and second conductive layers forming a conductor adjacent one of said spacers, said second conductive layer having a second dopant at a second dopant concentration formed on said first conductive layer, said first dopant diffusivity being less than said second dopant, said first dopant forming by solid state diffusion a shallow diffusion region in said one of the lightly doped source/drain regions beneath said conductor having a dopant concentration greater than said one of the lightly doped source/drain regions, and said second dopant providing a graded dopant concentration in a portion of said one of the lightly doped source/drain regions by diffusing below and adjacent said shallow diffusion region; and

continuing processing to form said integrated circuit device.

33. The method of claim 32 wherein said shallow diffusion region diffuses partially beneath said one of said spacer.

34. The method of claim 32 further comprising burning in said integrated circuit and accepting said integrated circuit if it exhibits well-behaved I_d/V_d curves for all V_g sweeps.

35. A conductor for a semiconductor substrate, comprising:

a first conductive layer on said semiconductor substrate;

a first dopant within said first conductive layer;

a second conductive layer adjacent said first conductive layer; and

a second dopant within said second conductive layer.

36. The conductor of claim 35 further comprising a doped region of the substrate under the first conductive layer.

37. The conductor of claim 36 further comprising a graded doped region of the substrate under said doped region.

38. The conductor of claim 35 located adjacent a transistor.

39. The conductor of claim 35 having a thickness of about 100 to about 1000 Angstroms for the first conductive layer.

40. The conductor of claim 35 having a thickness of about 2000 to about 2500 Angstroms for the second conductive layer.

41. The conductor of claim 35 wherein said first conductive layer lines a contact opening.

42. The conductor of claim 35 wherein said first conductive layer has an average dopant concentration for ranging from about 1 E 19 to about 1 E 21 ions/cm^3 of said first dopant.

43. The conductor of claim 35 wherein said second conductive layer has an average dopant concentration ranging from about 1 E 19 to about 1 E 21 ions/cm^3 of said second dopant.

44. The conductor of claim 35 wherein said first dopant diffusivity is less than said second dopant.

45. The conductor of claim 36 wherein said doped region extends under the conductor to a depth of no greater than about 0.02 μm.

46. The conductor of claim 36 wherein said doped region extends partially under a spacer provided adjacent said transistor.

47. The conductor of claim 36 wherein a dopant concentration of said doped region concentration is greater than a dopant concentration a lightly doped region of said substrate.

48. The conductor of claim 35, wherein said first dopant comprises arsenic, antimony, or combinations thereof, and said second dopant comprises phosphorus.

49. The conductor of claim 35, wherein said first dopant and said second dopant each comprises boron, boron bifluoride, borane, or combination thereof.

50. A memory integrated circuit (IC) device having a channel region less than 0.18μm and a gate overlap less than 0.018μm, said device comprising:

multilayered doped conductor means addressing reliability of said memory IC device at burn-in which through diffusion created a shallow, dopant portion with high dopant concentration in an active area of said device beneath said conductor means and adjacent the channel region, said shallow, dopant portion being less susceptible to depletion of trapped charges in the channel region.

51. The device of claim 50, wherein said conductor means is a device feature selected from the group consisting of a plug, a capacitor bottom plate, a digitline contact, and an active area contact.

52. The device of claim 50, wherein said conductor means comprises a first conductive layer and a second conductive layer provided adjacent to said first conductive layer, said second conductive layer having a greater dopant concentration that said first conductive layer.

53. The device of claim 52, wherein said first conductive layer has a dopant.

54. A memory integrated circuit (IC) device having a channel region less than 0.18μm and a gate overlap less than 0.018μm, said device comprising:

a shallow, dopant portion with high dopant concentration in an active area of said device, said shallow, dopant portion being less susceptible to depletion of trapped charges in the channel region.

55. The device of claim 54, wherein said shallow, dopant portion is beneath a conductor and adjacent the channel region.

56. The device of claim 54 wherein said doped region extends to a depth of no greater than about 0.02 μm in said active region.

57. A method of addressing susceptible to depletion of trapped charges in a channel region of a semiconductor substrate, said method comprising:

providing a shallow, dopant portion in the semiconductor substrate adjacent the channel region.

58. The method of claim 57, wherein providing includes:

providing a first conductive layer on said semiconductor substrate;

proving a first dopant within said first conductive layer;

providing a second conductive layer adjacent said first conductive layer; and

a second dopant within said second conductive layer, said second dopant diffusivity being greater that said first dopant.